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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,323	10/20/2000	Sreenivas Rao	015113-0001 (B69413)	8848
20594	7590	02/13/2004	EXAMINER	
CHRISTOPHER J. ROURK AKIN, GUMP, STRAUSS, HAUER & FELD, L.L.P. P O BOX 688 DALLAS, TX 75313-0688			HENN, TIMOTHY J	
		ART UNIT	PAPER NUMBER	
		2612	S	
DATE MAILED: 02/13/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/693,323	RAO ET AL.	
Examiner	Art Unit		
Timothy J Henn	2612		

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### **Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 20 October 2000.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-20 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-20 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 20 October 2000 is/are: a)  accepted or b)  objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_.  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: \_\_\_\_\_.  
\_\_\_\_\_

## DETAILED ACTION

### ***Specification***

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
2. The use of the trademarks has been noted in this application. Trademarks should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Kyrmkski et al. ("A High Speed, 500 Frames/s, 1024 x 1024 CMOS Active Pixel Sensor").

#### **[claim 10]**

5. In regard to claim 10, note that Krymski et al. discloses a high-speed CMOS imaging system comprising:

a CMOS active pixel sensor generating pixel data (Figure 1);

a controller coupled to the CMOS active pixel sensor, the controller receiving the pixel data and generating pixel line data (Figure 1, "Digital Control"; Page 2, Paragraph 3); and

wherein the pixel line data is generated at a rate greater than one line every 15 microseconds (The office notes that if the sensor is capable of generating 500 frames every second, then 1 frame will be generated in 2 milliseconds. Considering the fact that there are 1024 lines in the sensor and a frame is generated every 2 milliseconds, the sensor will generate a single line every 2 ms/1024 lines or 1.95  $\mu$ s / line. This is well under the claimed limit of 15  $\mu$ s / line rate).

**[claim 11]**

6. In regard to claim 11, note that Krymski et al. discloses a high-speed CMOS imaging system wherein the controller further comprises a pixel shift system initiating a pixel readout sequence to start at a pixel series position (Pages 1 – 2, "Achieving high speed and high performance" section).

**[claim 12]**

7. In regard to claim 12, note that Krymski et al. discloses a high-speed CMOS imaging system wherein the controller further comprises a framing system generating frames of image data at a rate greater than one frame every 30 milliseconds (The office notes that a frame generating speed of 500 frames/s is equivalent to generating a frame every 2 milliseconds.

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 1-7, 13-15, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilella (US 6,681,038) in view of Krymski et al. ("A High Speed, 500 Frames/s, 1024 x 1024 CMOS Active Pixel Sensor").

**[claim 1]**

10. In regard to claim 1, note that Vilella discloses a system for inspecting components comprising:

an imaging system generating image data (Column 4, Lines 6-11);  
an image analysis system coupled to the imaging device, the image analysis system receiving the image data and generating image analysis data (Column 4, Lines 12-25); and  
wherein the imaging system generates the image data at a rate that allows the imaging device to be used for inspecting components (The office notes that in an inspection system such as the one used by Vilella, it is inherent to generate image data at a rate that allows the imaging device to be used for inspecting components).

Therefore, it can be seen that Vilella lacks a CMOS imaging device.

11. However, Vilella states that that "Inspection speed can be further increased by adding more and faster processors to either or both systems" referring to the camera and the image analysis system. Krymski et al. discloses a CMOS active pixel sensor which is capable of generating 500 frames/s as an alternative to CCD image sensors for use in cameras in applications where high-speed imaging ("Abstract" and "Introduction" sections). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the image sensor of Krymski et al. in the camera of Vilella to help increase the inspection speed of the overall system.

**[claim 2]**

12. In regard to claim 2, note that the CMOS imaging sensor of Krymski et al. is a CMOS active pixel sensor.

**[claim 3]**

13. In regard to claim 3, it can be seen that the combination of Vilella in view of Krymski et al. lacks an CMOS imaging sensor which is a Photobit model PB1024 CMOS active pixel sensor. However, no criticality is given for the specific use of the model PB1024 CMOS active pixel sensor, therefore It would have been obvious to one of ordinary skill in the art at the time the invention was made to use any image sensor which meets the minimum specifications required for inspecting components (Official Notice).

**[claim 4]**

14. In regard to claim 4, note that Vilella discloses an imaging system comprising a processor coupled to the image analysis system (Column 4, Lines 48-55), the processor

operating one or more additional software systems used for image data analysis (Column 4, Lines 54-55). Therefore, it can be seen that Vilella in view of Krymski et al. lacks an imaging system which is an embedded imaging system.

15. However, it is well known in the microelectronics art that individual systems can be combined into embedded systems to save space. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the imaging system of Vilella in view of Krymski et al. an embedded imaging system (Official Notice).

**[claim 5]**

16. In regard to claim 5, note that Vilella discloses an imaging system which further comprises an image analysis controller receiving pixel data from a sensor and generating the image data from the pixel data (Column 4, Lines 6-11).

**[claim 6]**

17. In regard to claim 6, note that Krymski et al. discloses a CMOS imaging sensor that generates lines of image data at a speed greater than one line every 15.6 microseconds (The office notes that if the sensor is capable of generating 500 frames every second, then 1 frame will be generated in 2 milliseconds. Considering the fact that there are 1024 lines in the sensor and a frame is generated every 2 milliseconds, the sensor will generate a single line every 2 ms/1024 lines or 1.95  $\mu$ s / line. This is well under the claimed limit of 15  $\mu$ s / line rate).

**[claim 7]**

18. In regard to claim 7, see the discussion of claim 12.

**[claim 13]**

19. In regard to claim 13, note that Vilella discloses a method for generating image data of a component for use in inspecting the components comprising an imaging system generating image data (Column 4, Lines 6-11). Therefore, it can be seen that Vilella lacks an imaging system which is a CMOS imaging system, a step of transferring the pixel data as a plurality of pixel lines, and a step of assembling the pixel lines into a frame wherein the frame is assembled in less than 30 milliseconds.

20. However, Vilella states that that "Inspection speed can be further increased by adding more and faster processors to either or both systems" referring to the camera and the image analysis system. Krymski et al. discloses a CMOS active pixel sensor which is capable of generating 500 frames/s (or 1 frame every 2 microseconds) as an alternative to CCD image sensors for use in cameras in applications where high-speed imaging ("Abstract" and "Introduction" sections). Krymski et al. also discloses the transferring pixel data as a plurality of pixel lines ("Achieving high speed and high performance" section) and assembling the pixel lines into a frame. Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the CMOS active pixel sensor of Krymski et al. with the component inspection method of Vilella to achieve a component inspection method capable of higher inspection speeds than prior art systems.

**[claim 14]**

21. In regard to claim 14, note that the method of generating pixel of Krymski et al. uses a CMOS imaging system further comprising a CMOS active pixel sensor.

**[claim 15]**

22. In regard to claim 15, see the previous discussion of claim 3.

**[claim 19]**

23. In regard to claim 19, it is noted that Vilella in view of Krymski et al. lacks a method of assembling pixel lines into a frame that further comprises reading a first frame following the generation of a reset command. However, it is well known in the art to reset a sensor array prior to the generation of a frame to remove any signal charge which may have remained in the image sensor pixels prior to frame generation (Official Notice). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a reset command prior to the assembling of the pixel lines into a frame.

**[claim 20]**

24. In regard to claim 20, note that the image sensor of Krymski et al. can assemble a frame at different frame rates, from 15 f/s (66 ms/f) to 574 f/s (1.8  $\mu$ s/f). Therefore it can clearly be seen that the image sensor of Krymski et al. is capable of assembling a frame in the claimed 13.5 milliseconds. Official Notice is given that It would have been obvious to one of ordinary skill in the art at the time the invention was made to generate a frame every 13.5 milliseconds if required by the component inspection system of Vilella to achieve the desired results of component inspection.

25. Claims 8, 9 and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vilella (US 6,681,038) in view of Krymski et al. ("A High Speed, 500 Frames/s, 1024 x 1024 CMOS Active Pixel Sensor") as applied to claim 13 above, and further in view of Clark et al. (US 6,515,701).

**[claim 8]**

26. In regard to claim 8, note that Vilella in view of Krymski et al. discloses a method which meets the requirements set forth in claim 1 as discussed above. Therefore, it can be seen Vilella in view of Krymski et al. lacks a pixel shift system that enables a readout sequence to start at a pixel series position that reduces noise and improves signal quality.

27. Clark et al. teaches the use of a rolling shutter system which starts readout at a predetermined position, that can be used for reading out partial frames or specific areas of interest within the image sensor area (Column 7, Line 66 – Column 8, Line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of Clark et al. with the CMOS imaging system of Vilella in view of Krymski et al. to allow readout of only areas of interest on the image sensor array (The office notes that by only reading out a small area of the array, less noise will be read out).

**[claim 9]**

28. In regard to claim 9, note that the readout system of Clark et al. enables readout to start at any position, including a fifth pixel position (Column 7, Line 66 – Column 8,

Line 8).

**[claim 16]**

29. In regard to claim 16, note that Vilella in view of Krymski et al. discloses a method which meets the requirements set forth in claim 13 as discussed above. Therefore, it can be seen that Vilella in view of Krymski et al. lacks a transfer systems which generates a reset command, initiates a pixel line at the next clock cycle after the reset command, waits a predetermined number of clock cycles to generate a next pixel line wherein the predetermined number of clock cycles is less than 208 clock cycles.

30. Clark et al. discloses a rolling shutter system of pixel data readout which resets a number of lines, and after a set number of lines has been reset initiates a readout of the first line reset(Column 7, Line 9-16). The system of Clark et al. inherently waits a number of predetermined clock cycles between each readout line, which can be changed depending on the total exposure time the user desires (Column 7, Lines 50-65). Clark et al. discloses that such a system allows for improved control of exposure time of pixels in CMOS image sensors (Column 2, Lines 55-61). Therefore, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of Clark et al. with the method of Vilella in view of Krymski et al. to allow for improved control over exposure times in the CMOS imaging system.

**[claim 17]**

31. In regard to claim 8, note that Vilella in view of Krymski et al. discloses a method which meets the requirements set forth in claim 13 as discussed above. Therefore, it can be seen Vilella in view of Krymski et al. lacks a method that transfers the pixel data

as a plurality of pixel lines further comprising initiating a read sequence for each of the pixel lines at a predetermined pixel series position.

32. Clark et al. teaches the use of a rolling shutter method which starts readout at a predetermined position, that can be used for reading out partial frames or specific areas of interest within the image sensor area (Column 7, Line 66 – Column 8, Line 8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the system of Clark et al. with the method of Vilella in view of Krymski et al. to allow readout of only areas of interest on the image sensor array (The office notes that by only reading out a small area of the array, less noise will be read out).

**[claim 18]**

33. In regard to claim 18, note that the system of Clark et al. readout of a CMOS image sensor. The office notes that if an entire image array is readout, it is inherent that a read sequence will be initiated at a fourth pixel series position of each pixel line.

***Conclusion***

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Fossum et al.	"High Speed CMOS Imaging"
Fossum	"Active Pixel Sensors: Are CCD's Dinosaurs?"
Bechtel et al.	US 5,990,469
Pain et al.	US 6,519,371

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J Henn whose telephone number is (703) 305-8327. The examiner can normally be reached on M-F 7:30 AM - 5:00 PM, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy R Garber can be reached on (703) 305-4929. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJH  
2/9/2004



NGOC YEN VU  
PRIMARY EXAMINER